In the Specification

Please amend the specification of this application as follows:

Between paragraphs [0018] and [0019] insert paragraphs [0018a] and [0018b] as follows:

--[0018a] **Fig. 5** illustrates the difference in transistor width between first Wallace tree cells and second Wallace tree cells.

[0018b] **Fig. 6** illustrates the difference in transistor width between first Booth decoder cells and second Booth decoder cells.--

Rewrite paragraph [0032] as follows:

--[0032] For example as illustrated in **Fig. 5**, Wallace tree 112 may comprise a plurality of Wallace tree cells 112a and Wallace tree 312 may comprise a plurality of Wallace tree cells (not shown). Some Wallace tree cells 112a, such as a plurality of first Wallace tree cells 112a1, may be included within at least one critical path of multiply-accumulate module 100, i.e., at least one critical path of multiply-accumulate module 100 may comprise at least one first Wallace tree cell 112a1. Nevertheless, other Wallace tree cells 112a, such as a plurality of second Wallace tree cell 112a2, may not be included in any critical paths of multiply-accumulate module 100, i.e., none of the critical paths of multiply-accumulate module 100 may comprise any second Wallace tree cell 112a2. Moreover, each first Wallace tree cell 112a1 may comprise a first Wallace tree circuit ~~(not shown)~~ 520, which may comprise a first plurality of components, such as a first plurality of transistors ~~(not shown)~~ 521 and 522. Similarly, each second Wallace tree cell 112a2 may comprise a second Wallace tree circuit ~~(not shown)~~ 510, which may comprise a second plurality of components, such as a second plurality of transistors ~~(not shown)~~

511 and 512. Nevertheless, in this embodiment, although the second Wallace tree circuit may be structurally the same as the first Wallace tree circuit, a width of at least one of the second plurality of transistors 511 and 512 may be less than a width of at least one of the first plurality of transistors 521 and 522. Specifically, the width of at least one of the second plurality of transistors 511 and 512 may be less than the width of its corresponding first transistor 521 and 522. Decreasing the width of at least one of the second plurality of transistors 511 and 512 relative to the width of at least one of the first plurality of transistors 521 and 522 may increase an amount of time that it takes for the electrical signal to travel through at least one second Wallace tree cell 112a2 relative to an amount of time that it takes for the electrical signal to travel through at least one first Wallace tree cell 112a1. Nevertheless, decreasing the width of at least one of the second plurality of transistors 511 and 512 relative to the width of at least one of the first plurality of transistors 521 and 522 also may decrease an amount of power consumed by at least one second Wallace tree cell 112a2 relative to an amount of power consumed by at least one first Wallace tree cell 112a1. Consequently, the width of at least one of the second plurality of transistors 511 and 512 may be selected such that the amount of time that it takes for the electrical signal to travel through at least one second Wallace tree cell 112a2 may be less than or equal to the amount of time that it takes the electrical signal to travel through at least one first Wallace tree cell 112a1. Moreover, decreasing the amount of power consumed by at least one second Wallace tree cell 112a2 also may decrease an amount of power consumed by multiply-accumulate module 100.--

Rewrite paragraph [0033] as follows:

--[0033] In an alternative embodiment of the present invention, the width of each of the second plurality of transistors 511 and 512 of at least one second Wallace tree cell 112a2 may be less than the width of each of the first plurality of transistors 521 and 522 of at least one first Wallace tree cell 112a1. In yet another embodiment, the width of each of the second plurality of transistors 511 and 512 of each second Wallace tree cell 112a2 may be less than the width of each of the first plurality of transistors 521 and 522 of each first Wallace tree cell 112a1. Moreover, in any of the above described embodiments, each first Wallace tree cell 112a1 and each second Wallace tree cell 112a2 may be powered by the same power supply (not shown). In addition, in any of the above-described embodiments, a least significant bit of Wallace tree 112 or a most significant bit of Wallace tree 112, or both, which may be positioned at a first end portion and a second end portion of Wallace tree 112, respectively, may be a second Wallace tree cell 112a2. Similarly, in this embodiment, the least significant bit of Wallace tree 112 or the most significant bit of Wallace tree 112, or both, may not be a first Wallace tree cell 112a1, such that each first Wallace tree cell 112a1 may be positioned between second Wallace tree cells 112a2. Moreover, it will be understood by those of ordinary skill in the art that any of the above-described embodiments of the present invention may be applied to parallel multiplier 300.--

Rewrite paragraph [0034] as follows:

--[0034] Similarly as illustrated in **Fig. 6**, Booth decoder 110 may comprise a plurality of Booth decoder cells 110a and Booth decoder 310 may comprise a plurality of Booth decoder cells (not shown). Some Booth decoder cells 110a, such as a plurality of first Booth decoder cells 110a1, may be included within at least one critical path of multiply-accumulate module 100, i.e., at least

one critical path of multiply-accumulate module 100 may comprise at least one first Booth decoder cell 110a1. Nevertheless, other Booth decoder cells 110a, such as a plurality of second Booth decoder cell 110a2, may not be included in any critical paths of multiply-accumulate module 100, i.e., none of the critical paths of multiply-accumulate module 100 may comprise any second Booth decoder cell 110a2. Moreover, each first Booth decoder cell 110a1 may comprise a first Booth decoder circuit ~~(not shown)~~ 620, which may comprise a first plurality of components, such as a first plurality of transistors ~~(not shown)~~ 621 and 622. Similarly, each second Booth decoder cell 110a2 may comprise a second Booth decoder circuit ~~(not shown)~~ 610, which may comprise a second plurality of components, such as a second plurality of transistors ~~(not shown)~~ 611 and 612. Nevertheless, in this embodiment, although the second Booth decoder circuit 610 may be structurally the same as the first Booth decoder circuit 620, a width of at least one of the second plurality of transistors 611 and 612 may be less than a width of at least one of the first plurality of transistors 621 and 622. Specifically, the width of at least one of the second plurality of transistors 611 and 612 may be less than the width of its corresponding first transistor 621 and 622. Decreasing the width of at least one of the second plurality of transistors 611 and 612 relative to the width of at least one of the first plurality of transistors 621 and 622 may increase an amount of time that it takes for the electrical signal to travel through at least one second Booth decoder cell 110a2 relative to an amount of time that it takes for the electrical signal to travel through at least one first Booth decoder cell 110a1. Nevertheless, decreasing the width of at least one of the second plurality of transistors 611 and 612 relative to the width of at least one of the first plurality of transistors 621 and 622 also may decrease an amount of power consumed by at least one second Booth decoder cell 110a2 relative

to an amount of power consumed by at least one first Booth decoder cell 110a1. Consequently, the width of at least one of the second plurality of transistors 611 and 612 may be selected such that the amount of time that it takes for the electrical signal to travel through at least one second Booth decoder cell 110a2 may be less than or equal to the amount of time that it takes the electrical signal to travel through at least one first Booth decoder cell 110a1. Moreover, decreasing the amount of power consumed by at least one second Booth decoder cell 110a2 also may decrease an amount to power consumed by multiply-accumulate module 100.--

Rewrite paragraph [0035] as follows:

--[0035] In an alternative embodiment of the present invention, the width of each of the second plurality of transistors 611 and 612 of at least one second Booth decoder cell 110a2 may be less than the width of each of the first plurality of transistors 621 and 622 of at least one first Booth decoder cell 110a1. In yet another embodiment, the width of each of the second plurality of transistors 611 and 612 of each second Booth decoder cell 110a2 may be less than the width of each of the first plurality of transistors 621 and 622 of each first Booth decoder cell 110a1. Moreover, in any of the above described embodiments, each first Booth decoder cell 110a1 and each second Booth decoder cell 110a2 may be powered by the same power supply (not shown). In addition, in any of the above-described embodiments, a least significant bit of Booth decoder 110 or a most significant bit of Booth decoder 110, or both, which may be positioned at a first end portion and a second end portion of Booth decoder 110, respectively, may be a second Booth decoder cell 110a2. Similarly, in this embodiment, the least significant bit of Booth decoder 110 or the most significant bit of Booth decoder 110, or both, may not be a first Booth decoder cell 110a1, such that each first Booth decoder cell

110a1 may be positioned between second Booth decoder cells 110a2. Moreover, it will be understood by those of ordinary skill in the art that each of the above-described embodiments of the present invention may be used in combination with any other embodiment or embodiments of the present invention, and also may be applied to parallel multiplier 300.--

Rewrite paragraph [0036] as follows:

--[0036] In another embodiment of the present invention, a method of designing a multiply-accumulate module 100 may comprise the step of providing a multiply-accumulate core 120, which may comprise the steps of providing a plurality of Booth encoder cells 104a, and connecting a plurality of Booth decoder cells 110a to at least one Booth encoder cell 104a. Providing multiply-accumulate core 120 also may comprise the step of connecting a plurality of Wallace tree cells 112a to at least one Booth decoder cell 110a. Moreover, in this embodiment, at least one first cell, which may be at least one first Wallace tree cell 112a1 or at least one first Booth decoder cell 110a1, or any combination thereof, may comprise a first plurality of transistors (521 and 522, or 621 and 622). In addition, at least one second cell, which may be at least one second Wallace tree cell 112a2 or at least one second Booth decoder cell 110a2, or any combination thereof, may comprise a second plurality of transistors (511 and 512, or 611 and 612). Moreover, at least one critical path of multiply-accumulate module 100 may comprise the at least one first cell. The method further may comprise the steps of selecting a first width for at least one of the first plurality of transistors (521 and 522, or 621 and 622), and selecting a second width for at least one of the second plurality of transistors (511 and 512, or 611 and 612), which is less than the first width. Specifically, the width of at least one of the second plurality of transistors (511 and 512, or 611 and

612) may be selected such that an amount of time that it takes for an electrical signal to travel through the at least one second cell may be less than or equal to an amount of time that it takes the electrical signal to travel through the at least one first cell.--

Rewrite paragraph [0037] as follows:

--[0037] In yet another embodiment of the present invention, a method of designing a parallel multiplier may comprise the step of providing a parallel multiplier core 320, which may comprise the steps of providing a plurality of Booth encoder cells (not shown), and connecting a plurality of Booth decoder cells (not shown) to at least one Booth encoder cell (not shown). Providing parallel multiplier core 320 also may comprise the step of connecting a plurality of Wallace tree cells (not shown) to at least one Booth decoder cell (not shown). Moreover, in this embodiment, at least one first cell, which may be at least one first Wallace tree cell (not shown) or at least one first Booth decoder cell (not shown), or any combination thereof, may comprise a first plurality of transistors (521 and 522, or 621 and 622). In addition, at least one second cell, which may be at least one second Wallace tree cell (not shown) or at least one second Booth decoder cell (not shown), or any combination thereof, may comprise a second plurality of transistors (511 and 512, or 611 and 612). Moreover, at least one critical path of multiply-accumulate module 300 may comprise the at least one first cell. The method further may comprise the steps of selecting a first width for at least one of the first plurality of transistors (521 and 522, or 621 and 622), and selecting a second width for at least one of the second plurality of transistors (511 and 512, or 611 and 612), which is less than the first width. Specifically, the width of at least one of the second plurality of transistors (511 and 512, or 611 and 612) may be selected such that an amount of time that it takes for an electrical signal to travel

through the at least one second cell may be less than or equal to an amount of time that it takes the electrical signal to travel through the at least one first cell.--